Claim listing, showing amendments

Claims 1-15 (Cancelled)

16. (Currently Amended) A method, using a packet transmitter, comprising the steps of:

storing input data intended for a receiver, as stored data;

demultiplexing the stored data into a plurality of sub-data-sequence channels;

spread-spectrum processing the plurality of sub-data-sequence channels by a plurality of chip-sequence signals, respectively, thereby generating a plurality of spread-spectrum channels, with each of the plurality of chip-sequence signals different from other chip-sequence signals in the plurality of chip-sequence signals;

combining the plurality of spread-spectrum channels as a multichannel-spread-spectrum signal;

generating a header comprising a header-symbol-sequence signal **comprising a predefined sequence of symbols** spread-spectrum processed with a chip-sequence signal;

concatenating said header to the multichannel-spread-spectrum signal, thereby generating a packet-spread-spectrum signal intended for the receiver; and

transmitting on a carrier frequency using radio waves, the packet-spread-spectrum signal over a communications channel.

17. (Previously Presented) The method as set forth in claim 16, further including, between the steps of storing and demultiplexing, encoding the stored data as encoded data, with the step of demultiplexing the stored data including the step of demultiplexing the encoded data into the plurality of sub-data-sequence channels.

18. (Previously Presented) The method as set forth in claim 16, further including, between the steps of storing and demultiplexing, scrambling the stored data as encoded data, with the step of demultiplexing the stored data including the step of demultiplexing the encoded data into the plurality of sub-data-sequence channels.

19. (Previously Presented) The method as set forth in claim 16, further including, between the steps of storing and demultiplexing, encrypting the stored data as encoded data, with the step of demultiplexing the stored data including the step of demultiplexing the encoded data into the plurality of sub-data-sequence channels.

20. (Previously Presented) The method as set forth in claim 16, with the step of spread-spectrum processing including the step of multiplying the plurality of sub-data-sequence signals by the plurality of chip-sequence signals, respectively, thereby generating the plurality of spread-spectrum channels, with each chip-sequence signal in the plurality of chip-sequence signals different from other chip-sequence signals in the plurality of chip-sequence signals.

21. (Previously Presented) The method as set forth in claim 16, with the step of spread-spectrum processing including the step of multiplying the plurality of sub-data-sequence signals by the plurality of chip-sequence signals, respectively, thereby generating the plurality of spread-spectrum channels, with each chip-sequence signal in the plurality of chip-sequence signals orthogonal with respect to other chip-sequence signals in the plurality of chip-sequence signals.

22. (Previously Presented) The method as set forth in claim 16, with the step of combining including the step of algebraically combining the plurality of spread-spectrum channels as the multichannel-spread-spectrum signal.

23. (Previously Presented) The method as set forth in claim 16, 20 or 21 with the step of concatenating including the step of concatenating the header to the multichannel-spread-spectrum signal at an initial point of the multichannel-spread-spectrum signal, thereby generating the packet-spread-spectrum signal.

24. (Previously Presented) The method as set forth in claim 16, 20 or 21, with the step of concatenating including the step of concatenating the header to the multichannel-spread-spectrum signal, with the header followed in time by the multichannel-spread-spectrum signal, thereby generating the packet-spread-spectrum signal.

25. (Previously Presented) The method as set forth in claim 16, 20 or 21, with the step of spread-spectrum processing including the step of outputting a respective chip-sequence signal of the plurality of chip-sequence signals in response to a respective sub-data-sequence signal of the plurality of sub-data-sequence signals, thereby generating the plurality of spread-spectrum channels, with each chip-sequence signal in the plurality of chip-sequence signals orthogonal with respect to other chip-sequence signals in the plurality of chip-sequence signals.

26. (Previously Presented) The method as set forth in claim 16, 20 or 21, with the step of spread-spectrum processing including the step of outputting a respective chip-sequence signal

of the plurality of chip-sequence signals in response to a respective data symbol in a sub-data-sequence signal of the plurality of sub-data-sequence signals, thereby generating the plurality of spread-spectrum channels, with each chip-sequence signal in the plurality of chip-sequence signals orthogonal with respect to other chip-sequence signals in the plurality of chip-sequence signals.

27. (Currently Amended) A packet transmitter comprising:

transmitter-memory means for storing input data intended for a receiver, as stored data;

demultiplexer means, coupled to said transmitter memory means, for demultiplexing the stored data into a plurality of sub-data-sequence channels;

spread-spectrum means, coupled to said demultiplexer means, for spread-spectrum processing the plurality of sub-data-sequence signals by a plurality of chip-sequence signals, respectively, thereby generating a plurality of spread-spectrum channels, with each of the plurality of chip-sequence signals different from other chip-sequence signals in the plurality of chip-sequence signals;

combiner means, coupled to said spread-spectrum means, for combining the plurality of spread-spectrum channels as a multichannel-spread-spectrum signal;

header means, coupled to said combiner means, for concatenating a header to the multichannel-spread-spectrum signal, thereby generating a packet-spread-spectrum signal intended for the receiver, the header comprising a header-symbol-sequence signal **comprising a predefined sequence of symbols** spread-spectrum processed with a chip-sequence signal; and

transmitter means, coupled to said header means, for transmitting on a carrier frequency using radio waves, the packet-spread-spectrum signal over a communications channel.

28. (Previously Presented) The packet transmitter as set forth in claim 27, further including encoder means, coupled between said transmitter-memory means and said demultiplexer means, for encoding the stored data as encoded data, with said demultiplexer means including means for demultiplexing the encoded data into the plurality of sub-data-sequence channels.

29. (Previously Presented) The packet transmitter as set forth in claim 27, further including encoder means, coupled between said transmitter-memory means and said demultiplexer means, for scrambling the stored data as encoded data, with said demultiplexer means including means for demultiplexing the encoded data into the plurality of sub-data-sequence channels.

30. (Previously Presented) The packet transmitter as set forth in claim 27, further including encoder means, coupled between said transmitter-memory means and said demultiplexer means, for encrypting the stored data as encoded data, with said demultiplexer means including means for demultiplexing the encoded data into the plurality of sub-data-sequence channels.

31. (Previously Presented) The packet transmitter as set forth in claim 27, with said spread-spectrum means including multiplying means for multiplying the plurality of sub-data-sequence signals by the plurality of chip-sequence signals, respectively, thereby generating the plurality of spread-spectrum channels, with each chip-sequence signal in the plurality of chip-

sequence signals different from other chip-sequence signals in the plurality of chip-sequence signals.

32. (Previously Presented) The packet transmitter as set forth in claim 27, with said spread-spectrum means including multiplying means for multiplying the plurality of sub-data-sequence signals by the plurality of chip-sequence signals, respectively, thereby generating the plurality of spread-spectrum channels, with each chip-sequence signal in the plurality of chip-sequence signals orthogonal with respect to other chip-sequence signals in the plurality of chip-sequence signals.

33. (Previously Presented) The packet transmitter as set forth in claim 27, with said combiner means including means for algebraically combining the plurality of spread-spectrum channels as the multichannel-spread-spectrum signal.

34. (Previously Presented) The packet transmitter as set forth in claim 27, 31 or 32, with said header means including means for concatenating the header to the multichannel-spread-spectrum signal at an initial point of the multichannel-spread-spectrum signal, thereby generating the packet-spread-spectrum signal.

35. (Previously Presented) The packet transmitter as set forth in claim 27, 31 or 32, with said header means including means for concatenating the header to the multichannel-spread-spectrum signal, with the header followed in time by the multichannel-spread-spectrum signal, thereby generating the packet-spread-spectrum signal.

36. (Previously Presented) The packet transmitter as set forth in claim 27, 31 or 32, with said spread-spectrum means including spread-spectrum-memory means for outputting a respective chip-sequence signal of the plurality of chip-sequence signals in response to a respective sub-data-sequence signal of the plurality of sub-data-sequence signals, thereby generating the plurality of spread-spectrum channels, with each chip-sequence signal in the plurality of chip-sequence signals orthogonal with respect to other chip-sequence signals in the plurality of chip-sequence signals.

37. (Previously Presented) The packet transmitter as set forth in claim 27, 31 or 3, with said spread-spectrum means including spread-spectrum-memory means for outputting a respective chip-sequence signal of the plurality of chip-sequence signals in response to a respective data symbol in a sub-data-sequence signal of the plurality of sub-data-sequence signals, thereby generating the plurality of spread-spectrum channels, with each chip-sequence signal in the plurality of chip-sequence signals orthogonal with respect to other chip-sequence signals in the plurality of chip-sequence signals.

38. (Currently Amended) A packet transmitter comprising:

a transmitter memory for storing input data intended for a receiver, as stored data;

a demultiplexer, coupled to said transmitter memory, for demultiplexing the stored data into a plurality of sub-data-sequence channels;

spread-spectrum means, coupled to said demultiplexer, for spread-spectrum processing the plurality of sub-data-sequence signals by a plurality of chip-sequence signals, respectively,

thereby generating a plurality of spread-spectrum channels, with each of the plurality of chip-sequence signals different from other chip-sequence signals in the plurality of chip-sequence signals;

a combiner, coupled to said spread-spectrum means, for combining the plurality of spread-spectrum channels as a multichannel-spread-spectrum signal;

a header device, coupled to said combiner, for concatenating a header to the multichannel-spread-spectrum signal, thereby generating a packet-spread-spectrum signal intended for the receiver, the header comprising a header-symbol-sequence signal **comprising a predefined sequence of symbols** spread-spectrum processed with a chip-sequence signal; and

a transmitter subsystem, coupled to said header device, for transmitting on a carrier frequency using radio waves, the packet-spread-spectrum signal over a communications channel.

39. (Previously Presented) The packet transmitter as set forth in claim 38, further including, between said transmitter memory and said demultiplexer, an encoder for encoding the stored data as encoded data, with the demultiplexer including means for demultiplexing the encoded data into the plurality of sub-data-sequence channels.

40. (Previously Presented) The method as set forth in claim 38, further including, between said transmitter memory and said demultiplexer, an encoder for scrambling the stored data as encoded data, with the demultiplexer including means for demultiplexing the encoded data into the plurality of sub-data-sequence channels.

41. (Previously Presented) The packet transmitter as set forth in claim 38, further including, between said transmitter memory and said demultiplexer, an encoder for encrypting the stored data as encoded data, with the demultiplexer including means for demultiplexing the encoded data into the plurality of sub-data-sequence channels.

42. (Previously Presented) The packet transmitter as set forth in claim 38, with said spread-spectrum means including a plurality of product devices for multiplying the plurality of sub-data-sequence signals by the plurality of chip-sequence signals, respectively, thereby generating the plurality of spread-spectrum channels, with each chip-sequence signal in the plurality of chip-sequence signals different from other chip-sequence signals in the plurality of chip-sequence signals.

43. (Previously Presented) The packet transmitter as set forth in claim 38, with said spread-spectrum means including a plurality of product devices for multiplying the plurality of sub-data-sequence signals by the plurality of chip-sequence signals, respectively, thereby generating the plurality of spread-spectrum channels, with each chip-sequence signal in the plurality of chip-sequence signals orthogonal with respect to other chip-sequence signals in the plurality of chip-sequence signals.

44. (Previously Presented) The packet transmitter as set forth in claim 38, 42 or 43, with said header device including means for concatenating the header to the multichannel-spread-spectrum signal at an initial point of the multichannel-spread-spectrum signal, thereby generating the packet-spread-spectrum signal.

45. (Previously Presented) The packet transmitter as set forth in claim 38, 42 or 43, with said header device including means for concatenating the header to the multichannel-spread-spectrum signal, with the header followed in time by the multichannel-spread-spectrum signal, thereby generating the packet-spread-spectrum signal.

46. (Previously Presented) The packet transmitter as set forth in claim 38, 42 or 43, with said spread-spectrum means including a memory for outputting a respective chip-sequence signal of the plurality of chip-sequence signals in response to a respective sub-data-sequence signal of the plurality of sub-data-sequence signals, thereby generating the plurality of spread-spectrum channels, with each chip-sequence signal in the plurality of chip-sequence signals orthogonal with respect to other chip-sequence signals in the plurality of chip-sequence signals.

47. (Previously Presented) The packet transmitter as set forth in claim 38, 42 or 43, with said spread-spectrum means including a memory for outputting a respective chip-sequence signal of the plurality of chip-sequence signals in response to a respective data symbol in a sub-data-sequence signal of the plurality of sub-data-sequence signals, thereby generating the plurality of spread-spectrum channels, with each chip-sequence signal in the plurality of chip-sequence signals orthogonal with respect to other chip-sequence signals in the plurality of chip-sequence signals.

48. (Previously Presented) The method as set forth in claim 16, 20 or 21 with the step of outputting a respective chip-sequence signal of the plurality of chip-sequence signals in response

to a respective data symbol in a sub-data-sequence signal of the plurality of sub-data-sequence signals, thereby generating the plurality of spread-spectrum channels, with each chip-sequence signal in the plurality of the chip-sequence signals different from other chip-sequence signals in the plurality of chip-sequence signals.

49. (Previously Presented) The packet transmitter as set forth in claim 27, 31 or 32, with said spread-spectrum means including spread-spectrum-memory means for outputting a respective chip-sequence signal of the plurality of chip-sequence signals in response to a respective data symbol in a sub-data-sequence signal of the plurality of sub-data-sequence signals, thereby generating the plurality of spread-spectrum channels, with each chip-sequence signal in the plurality of the chip-sequence signals different from other chip-sequence signals in the plurality of chip-sequence signals.

50. (Previously Presented) The packet transmitter as set forth in claim 38, 42 or 43, with said spread-spectrum means including spread-spectrum-memory means for outputting a respective chip-sequence signal of the plurality of chip-sequence signals in response to a respective data symbol in a sub-data-sequence signal of the plurality of sub-data-sequence signals, thereby generating the plurality of spread-spectrum channels, with each chip-sequence signal in the plurality of the chip-sequence signals different from other chip-sequence signals in the plurality of chip-sequence signals.